DETAILED ACTION

This Office Action is responsive to the Applicant's communication filed 03/05/2007. In virtue of this communication, claims 1-16 are pending in the instant application.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gilbert (U.S. Patent No. 4,156,283) in view of Hieda (U.S. Publication No. 2002/0011612 A1) and Tadahiro et al (Japanese Publication No. 2002-261091;

hereinafter referred to as Tadahiro, all prosecution is based on machine translations).

With respect to claim 1, Gilbert discloses in Figure 2, a mixer circuit, comprising at least a differential pair transistors [10],[12] for inputting a first frequency signal or a second frequency signal and generating a third frequency signal by multiplying the first frequency signal and the second frequency signal (see Column 8, lines 10-55).

Gilbert fails to disclose each transistor is a MIS transistor comprising: a semiconductor substrate for comprising a first crystal plane as a principal plane; a semiconductor structure, formed as a part of the semiconductor substrate, for comprising a pair of sidewall planes defined by the second crystal plane different from the first crystal plane and a top plane defined by the third crystal plane different from the second crystal plane; a gate insulator of uniform thickness for covering the principal plane, the sidewall planes and the top plane; a gate electrode for continuously covering the principal plane, the sidewall planes and the top plane on top of the gate insulator; and a single conductivity type diffusion region formed in one side and the other side of the gate electrode in the semiconductor substrate and the semiconductor structure and continuously extending along the principal plane, the sidewall planes and the top plane.

Hieda teaches each transistor is a MIS transistor (see Paragraph [0174]) comprising: a semiconductor substrate; a semiconductor structure (gate electrode), formed as a part of the semiconductor substrate, for comprising a pair of sidewall planes(see Paragraph [0029]); a gate insulator of uniform thickness for covering the principal plane, the sidewall planes and the top plane (see Paragraph [0029]); a gate electrode for continuously covering the principal plane (substrate) (see Paragraph

[0029]), the sidewall planes and the top plane on top of the gate insulator; and a single conductivity type diffusion region [24] (see Paragraph [0213]) formed in one side and the other side of the gate electrode in the semiconductor substrate and the semiconductor structure and continuously extending along the principal plane, the sidewall planes and the top plane (see Figure 29 and Paragraph [0214]).

Hieda fails to disclose the semiconductor substrate comprising a first crystal plane as a principal plane, a semiconductor structure, comprising the pair of sidewall planes defined by the second crystal plane different from the first crystal plane and a top plane defined by the third crystal plane different from the second crystal plane.

Tadahiro discloses the semiconductor substrate comprising a first crystal plane as a principal plane, a semiconductor structure, comprising the pair of sidewall planes defined by the second crystal plane different from the first crystal plane and a top plane defined by the third crystal plane different from the second crystal plane (see Paragraph [0022]).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement the circuit of Gilbert with the MIS transistor type having the structure as taught by Hieda in order to produce a transistor type with modifiable threshold voltage, allowing for a modifiable work function of the transistor (see Hieda, Page 10, Paragraph [208]) Furthermore, it would have been obvious to one of ordinary skill in the art at the time of invention to produce all semiconductor elements as disclosed by Tadahiro to produce the individual and unique desired crystal planes in order to augment the mixer circuit as disclosed by the combination of Gilbert and Hieda

in order to produce a highly efficient transistor integrated circuit with high permittivity gate dielectric films (see Tadahiro Paragraph [0022]).

With respect to claim 2, Gilbert discloses in Figure 2, a mixer circuit, comprising at least a differential pair transistors [10],[12] for inputting a first frequency signal or a second frequency signal and generating a third frequency signal by multiplying the first frequency signal and the second frequency signal (see Column 8, lines 10-55).

Gilbert fails to disclose a semiconductor substrate comprising a projecting part, of which the surfaces are at least two different crystal planes on a principal plane; a gate insulator for covering the surface of the projecting part; a gate electrode comprised by the gate insulator so as to be electrically insulated from the semiconductor substrate, and comprised on the surface of the projecting part; and a single conductivity type diffusion region formed in the projecting part facing each surface of the projecting part and individually formed in both side of the gate electrode.

Hieda discloses a semiconductor substrate comprising a projecting part (sidewall), a gate insulator for covering the surface of the projecting part; a gate electrode comprised by the gate insulator so as to be electrically insulated from the semiconductor substrate, and comprised on the surface of the projecting part (see Paragraph [0029]), and a single conductivity type diffusion region formed in the projecting part facing each surface of the projecting part and individually formed in both side of the gate electrode (see Paragraph [0213]).

Hieda fails to disclose that the surfaces of the projecting part are at least two different crystal planes on a principal plane

Tadahiro discloses that the surfaces of the projecting part are at least two different crystal planes on a principal plane (see Paragraph [0022]).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement the circuit of Gilbert with the MIS transistor type having the structure as taught by Hieda in order to produce a transistor type with modifiable threshold voltage, allowing for a modifiable work function of the transistor (see Hieda, Page 10, Paragraph [208]). Furthermore, it would have been obvious to one of ordinary skill in the art at the time of invention to produce all semiconductor elements as disclosed by Tadahiro to produce the individual and unique desired crystal planes in order to augment the mixer circuit as disclosed by the combination of Gilbert and Hieda in order to produce a highly efficient transistor integrated circuit with high permittivity gate dielectric films (see Tadahiro Paragraph [0022]).

With respect to claim 3, Gilbert discloses in Figure 2, a mixer circuit, comprising at least a differential pair transistors [10],[12] for inputting a first frequency signal or a second frequency signal and generating a third frequency signal by multiplying the first frequency signal and the second frequency signal (see Column 8, lines 10-55).

Gilbert fails to disclose a semiconductor substrate comprising at least two crystal planes; a gate insulator formed on at least two of the crystal planes of the semiconductor substrate; and a gate electrode formed on the semiconductor substrate sandwiching the gate insulator, in which when voltage is applied to the gate electrode, a channel width of a channel formed in the semiconductor substrate along with the gate insulator is represented by summation of each channel width of the channels

individually formed on said at least two crystal planes.

Hieda discloses a semiconductor substrate; a gate insulator formed on the semiconductor substrate; and a gate electrode formed on the semiconductor substrate sandwiching the gate insulator, in which when voltage is applied to the gate electrode (see Figures 7A, 7B, 8A, and 8B and Paragraph [0029]), a channel width of a channel formed in the semiconductor substrate along with the gate insulator is represented by summation of each channel width of the channels individually formed on said substrate (see Paragraph [0036]).

Hieda fails to disclose the substrate comprises at least two crystal planes.

Tadahiro discloses the semiconductor substrate comprises at least two crystal planes (see Paragraph [0022]).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement the circuit of Gilbert with the MIS transistor type having the structure as taught by Hieda in order to produce a transistor type with modifiable threshold voltage, allowing for a modifiable work function of the transistor (see Hieda, Page 10, Paragraph [208]). Furthermore, it would have been obvious to one of ordinary skill in the art at the time of invention to produce all semiconductor elements as disclosed by Tadahiro to produce the individual and unique desired crystal planes in order to augment the mixer circuit as disclosed by the combination of Gilbert and Hieda in order to produce a highly efficient transistor integrated circuit with high permittivity gate dielectric films (see Tadahiro Paragraph [0022]).

With respect to claim 4, the combination of Gilbert, Hieda and Tadahiro disclose

all material as disclosed in claims 1 and further discloses that the semiconductor substrate is a silicon substrate (see Hieda Page 7, Paragraph [0176]) and that a gate insulator on a surface of the silicon substrate, is formed by removing hydrogen in such a way that the surface of the silicon substrate is exposed to plasma of a prescribed inert gas, and the hydrogen content at the interface of the silicon substrate and the gate insulator is $10^{11}/cm^2$ or less in units of surface density (see Tadahiro Paragraph [0043]).

It would have been obvious to one of ordinary skill in the art at the time of invention to utilize the removal of hydrogen as taught by Tadahiro in order to lower the leakage of current of the mixer circuit as disclosed by the combination of Gilbert and Hieda (see Tadahiro, Paragraph [0017]-[0018]).

With respect to claim 5, the combination of Gilbert, Hieda, and Tadahiro disclose all material as disclosed in claims 2 and further discloses wherein the MIS transistor is characterized in: that the semiconductor substrate is a silicon substrate (see Hieda Page 7, Paragraph [0176]) and a gate insulator on a surface of the silicon substrate, is formed by removing hydrogen in such a way that the surface of the silicon substrate is exposed to plasma of a prescribed inert gas, and the hydrogen content at the interface of the silicon substrate and the gate insulator is $10^{11}/cm^2$ or less in units of surface density (see Tadahiro Paragraph [0043]).

With respect to claim 6, the combination Gilbert, Hieda, and Tadahiro disclose all material as disclosed in claims 3 and further discloses wherein the MIS transistor is characterized in: that the semiconductor substrate is a silicon substrate (see Hieda Page 7, Paragraph [0176]) and a gate insulator on a surface of the silicon substrate, is

formed by removing hydrogen in such a way that the surface of the silicon substrate is exposed to plasma of a prescribed inert gas, and the hydrogen content at the interface of the silicon substrate and the gate insulator is $10^{11}/cm^2$ or less in units of surface density (see Tadahiro Paragraph [0043]).

With respect to claim 7, the combination of Gilbert, Hieda, and Tadahiro disclose all material as disclosed in claim 4 and further discloses wherein said at least two crystal planes are any two different crystal planes from a (100) plane, a (110) plane and a (111) plane (see Tadahiro, Paragraph [0006]).

With respect to claim 8, the combination of Gilbert disclose all material as disclosed in claim 1 and further discloses wherein the mixer circuit is a Gilbert cell type circuit (see Column 1, lines 40-59; the patent discloses all elements of the Gilbert mixer circuit).

With respect to claim 9, the combination of Gilbert, Hieda, and Tadahiro disclose all material as disclosed in claim 1 and further discloses the circuit configuration of the mixer circuit is using the MIS transistors symmetrically (see Gilbert Column 4, lines 3-30).

With respect to claim 10, the combination of Gilbert, Hieda, and Tadahiro disclose all material as disclosed in claims 3 and further discloses the circuit configuration of the mixer circuit is using the MIS transistors symmetrically (see Gilbert Column 4, lines 3-30).

With respect to claim 11, the combination of Gilbert, Hieda, and Tadahiro disclose all material as disclosed in claim 1 and further discloses the mixer circuit used

as a receiver for the first frequency signal, which is a high-frequency signal, the second frequency signal, which is a local signal, and the third frequency signal, which is a low-frequency signal (see Gilbert Column 8, lines 35- column 9, line 4).

With respect to claim 12, the combination of Gilbert, Hieda, and Tadahiro disclose all material as disclosed in claims 3 and further discloses the mixer circuit used as a receiver for the first frequency signal, which is a high-frequency signal, the second frequency signal, which is a local signal, and the third frequency signal, which is a low-frequency signal (see Gilbert Column 8, lines 35- column 9, line 4).

With respect to claim 13, the combination of Gilbert, Hieda, and Tadahiro disclose all material as disclosed in claims 11 and further discloses wherein the low-frequency signal is used in a direct conversion receiving system where the signal is a base band signal Column 9, line 5-18).

With respect to claim 14, the combination of Gilbert, Hieda, and Tadahiro disclose all material as disclosed in claims 1 and further discloses a mixer circuit, comprising a CMOS transistor configured in an n-channel MOS transistor and a p-channel MOS transistor, wherein at least one of the n-channel MOS transistor or the p-channel MOS transistor comprises the MIS transistor of the mixer circuit according to claim 1 (see Hieda Paragraph [0407]).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement the CMOS transistors of Hieda within the mixer circuit of the combination of Gilbert and Tadahiro in order to suppress drive performance dispersion of the circuit transistors (see Hieda, Page 23, Paragraph [0419]).

With respect to claim 15, the combination of Gilbert, Hieda, and Tadahiro disclose all material as disclosed in claims 3 and further discloses a mixer circuit, comprising a CMOS transistor configured in an n-channel MOS transistor and a p-channel MOS transistor, wherein at least one of the n-channel MOS transistor or the p-channel MOS transistor comprises the MIS transistor of the mixer circuit according to claim 1 (see Hieda Paragraph [0407]).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement the CMOS transistors of Hieda within the mixer circuit of the combination of Gilbert and Tadahiro in order to suppress drive performance dispersion of the circuit transistors (see Hieda Page 23, Paragraph [0419]).

5. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gilbert (U.S. Patent No. 4,156,283) in view of Hieda (U.S. Publication No. 2002/0011612 A1) and Tadahiro et al (Japanese Publication No. 2002-261091; hereinafter referred to as Tadahiro) as applied to claims 1 and 14 above, and further in view of Nariyoshi (Japanese Publication No. 11-055096).

With respect to claim 16, the combination of Gilbert, Hieda, and Tadahiro disclose all material as disclosed in claim 14 but fails to disclose wherein element areas and current driving capacities of the p-channel MOS transistor and the n-channel MOS transistor closely agree with each other.

Nariyoshi teaches wherein element areas and current driving capacities of the p-channel MOS transistor and the n-channel MOS transistor closely agree with each other (see Paragraph [0024]-[0028]).

It would have been obvious to one of ordinary skill in the art at the time of invention to supplement the mixer circuit of the combination of Gilbert, Hieda, and Tadahiro with the system parameters as taught by Nariyoshi in order to shorten the signal input transition time to a gate (see Nariyoshi Paragraph [0023]).

Citation of Pertinent Art

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Anderson et al. (U.S. Patent No. 5,564,094) discloses a mixer circuit capable of receiving an output of an amplifier and multiplying it with an injection signal.

- De Loe, Jr. et al. (U.S. Patent No. 5,649,288) discloses a double balanced mixer circuit functioning as a modulation switch during an imbalance state for a multi-mode communication device.

- Kang (U.S. Patent No. 6,028,850) discloses a mixer circuit capable of receiving IF signals.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JONATHAN HAN whose telephone number is (571)270-7546. The examiner can normally be reached on Monday Through Friday 7:30 AM -5 PM EST, Alternate Fridays Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thuy V. Tran can be reached on (571)272-1828. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Thuy Vinh Tran/
Supervisory Patent Examiner, Art Unit 4176
02/26/2009

/JONATHAN HAN/
Examiner, Art Unit 4176